A 0.5-V 8-bit 10-Ms/s Pipelined ADC in 90-nm CMOS

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***Abstract*—This paper presents a pipelined analog-to-digital converter (ADC) operating from a 0.5-V supply voltage. The ADC uses true low-voltage design techniques that do not require any on-chip supply or clock voltage boosting. The switch OFF leakage in the sampling circuit is suppressed using a cascaded sampling technique. A front-end signal-path sample-and-hold amplifier (SHA) is avoided by using a coarse auxiliary sample and hold (S/H) for the sub-ADC and by synchronizing the sub-ADC and pipeline-stage sampling circuit. A 0.5-V operational transconductance amplifier (OTA) is presented that provides inter-stage amplification with an 8-bit performance for the pipelined ADC operating at 10 Ms/s. The chip was fabricated on a standard 90 nm CMOS technology and measures 1.2 mm $\times$ 1.2 mm. The prototype chip has eight identical stages and stage scaling was not used. It consumes 2.4 mW for 10-Ms/s operation. Measured peak SNDR is 48.1 dB and peak SFDR is 57.2 dB for a full-scale sinusoidal input. Maximal integral nonlinearity and differential nonlinearity are 1.19 and 0.55 LSB, respectively.**

***Index Terms*—Analog-to-digital converter (ADC), cascaded sampling, low-voltage operational transconductance amplifier (OTA), pipelined ADC, switch leakage, ultra-low-voltage analog circuits.**

I. Introduction

THE research goal of exploring ultra-low-voltage analog circuit design is motivated by several trends in integrated circuit design and semiconductor technologies and the applications they enable. System-on-a-chip (SOC) designs have made possible substantial cost and form factor reductions, in part since they integrate crucial analog interface circuits, such as analog-to-digital converters (ADCs), with digital computing and signal processing circuits on the same die. The interfaces only occupy a small fraction of the chip die and, for SOC designs, the technology selection and system design choices are mainly driven by digital circuit requirements. In the past decades, design techniques for analog interface circuits that are fully compatible with scaled standard digital CMOS technologies and do not require special technology options have been important enablers to continue ever more complex SOC designs (see, e.g., [1]). As the feature sizes in modern nanoscale CMOS technologies reduce, the maximum supply voltage also has to be reduced to maintain reliable device operation. The International Technology Roadmap for Semiconductors (ITRS) foresees that the supply voltage for low-power digital circuits will scale below 1 V for high-performance applications and down to 0.5 V for low-power applications within the next decade or so [2]. Additionally, the most energy-efficient operation of digital systems occurs for supply voltages between 0.3 and 0.5 V in deeply scaled technologies.

Scavenging the energy to operate circuits from the environment is desirable for applications such as wireless sensor nodes or ambient intelligence. e.g., if, due to space constraints, only one solar cell is available, the supply voltage is about 0.5 V [3], [4].

Pipelined ADCs are a popular choice for analog-to-digital conversion because of their attractive features of high operation speed, good resolution, and low power consumption. In this study, an 8-bit 10-Ms/s pipelined ADC is targeted with an aggressive low supply voltage of 0.5 V [5]. In prior work, several techniques have been developed to accommodate low-voltage analog circuit design such as the use of special low-$\mathrm{V_T}$ devices [6], [7], on-chip clock and gate voltage boosting [8]–[11], body driven circuits [12], [13], or switched-opamp [14]–[16] techniques. Low-$\mathrm{V_T}$ devices require extra masks during fabrication and thus result in higher cost. On-chip voltage boosting can lead to long-term reliability concerns, especially for nanoscale CMOS devices. Using the body terminal of a MOSFET offers the circuit designer a number of interesting circuit design opportunities, but the body transconductance $\mathrm{g_{mb}}$ is significantly smaller than the gate transconductance g_m, which can limit the attainable speed or noise performance. Switched-opamp techniques have been successfully used for very low-voltage designs but typically operate at a reduced operation frequency due to the amplifier turn-on times.

The work presented here is using true low-voltage design techniques to take full advantage of advanced CMOS technologies without resorting to special devices or on-chip voltage boosting. In Section II, the top-level design of the pipelined ADC is presented and the use of an auxiliary sample and hold for the sub-ADC is introduced. Cascaded sampling as a solution to address switch-off-state leakage is discussed in Section III. Section IV discusses the design of the 0.5-V operational transconductance amplifier (OTA). Experimental results are presented in Section V, followed by concluding remarks in Section VI.

II. Low-Voltage Pipelined ADC Design

A. Top-Level and Stage Design Considerations

In ultra-low-voltage analog design, one intrinsic challenge is the reduced available signal swing. It makes multi-bit stages not desirable due to comparator offset and hysteresis concerns.

Manuscript received August 27, 2007; revised October 22, 2007. This work was supported by Realtek Corporation. Chip prototype fabrication was provided by United Microelectronics Corporation.

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Digital Object Identifier 10.1109/JSSC.2008.917470

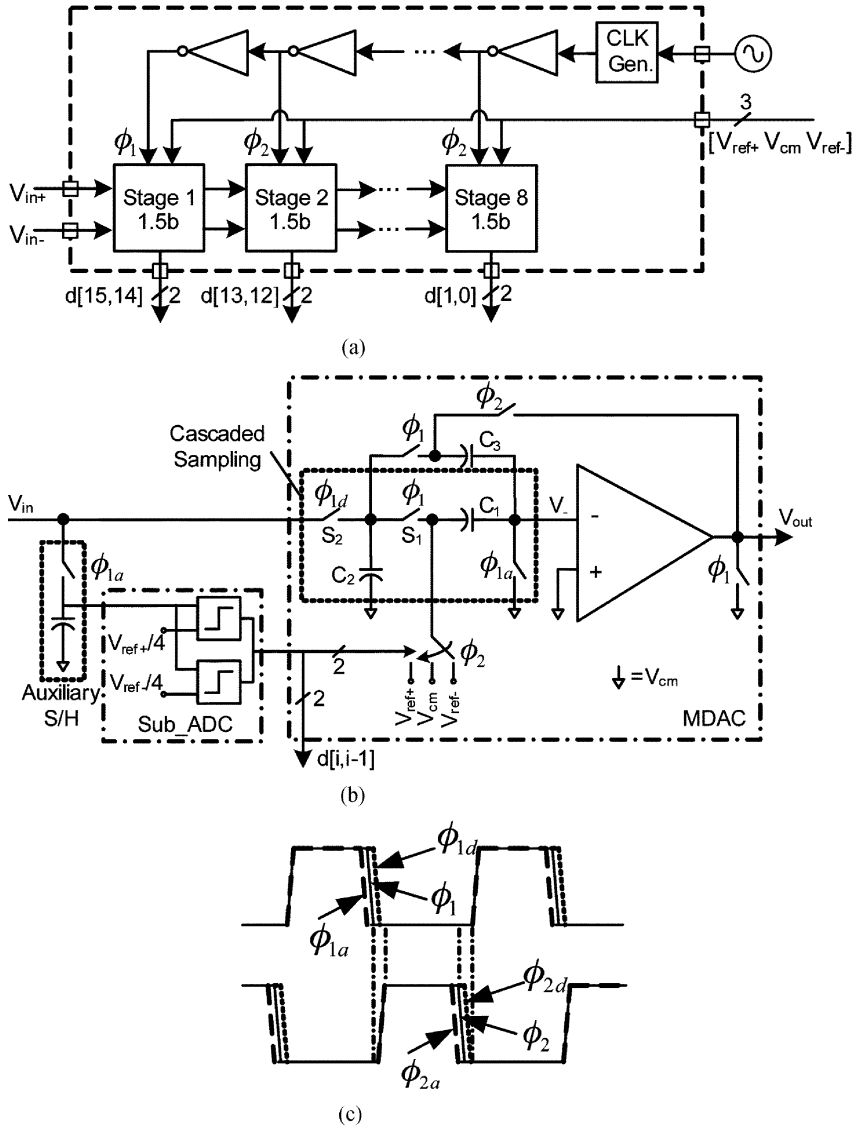

Fig. 1. (a) Block diagram of the pipeline ADC prototype chip and (b) single-ended version of one pipeline stage. (c) Nonoverlapping clock signals (ϕ_1, ϕ_2) and their advanced (ϕ_{1a}, ϕ_{2a}) and delayed versions used to minimize charge injection and clock feedthrough and to ensure accurate sampling.

Multi-bit stages further require a higher open-loop gain–bandwidth (GBW) for the residue amplifiers due to the small feedback factors in the stage. In this design, we use the 1.5-bit/stage architecture. Fig. 1(a) shows the block diagram of the converter chip prototype. To simplify the prototype design, the second through the eighth stages were kept identical to the first stage, which has the most stringent performance requirements. In a redesign, the power consumption can be reduced by applying progressive size and power scaling to the later stages. No sample-and-hold amplifier (SHA) is implemented in front of the pipelined ADC to save power and reduce noise. This is made possible by the introduction of an auxiliary sample and hold (S/H) for the sub-ADC, which will be presented later in this section. A single-ended diagram of a stage of the pipelined ADC is shown in Fig. 1(b) for clarity, but the actual chip implementation is fully differential. It consists of two comparators as sub-ADC and a multiplying digital-to-analog converter (MDAC) that performs signal sampling, subtraction, and residue amplification. A 400-mV peak-to-peak differential full-scale input swing is targeted, taking into account the typical available output swing of a 0.5-V OTA. The signal common-mode voltage is set to 250 mV and the reference voltages are 250 mV $\pm$ 100 mV. For an 8 bit accuracy level, the LSB of the ADC is still as large as 1.6 mV.

The choice of the size of the sampling capacitor is driven by the concern of keeping parasitic capacitors sufficiently small. To avoid an extra mask to realize the metal–insulator–metal (MIM) capacitors, an interdigitated metal1-through-metal6 capacitor with a unit size of 250 fF and an area of 130 μm^2 was custom designed and verified using electromagnetic simulations. In this design, four unit capacitors in a common-centroid layout for improved matching are used to realize the sampling capacitors C_1 and C_3. The RMS value of the thermal noise $\sqrt{\overline{v_{n,\mathrm{RMS}}^2}} = \sqrt{kT/C}$ for a 1 pF sampling capacitor is 64 μV$_{\mathrm{RMS}}$ and sufficiently small compared with one LSB value.

The on-chip clock generator generates two nonoverlapping clock signals ϕ_1 and ϕ_2 from an external clock reference. Each clock signal also has an advanced version ϕ_{1a} and delayed

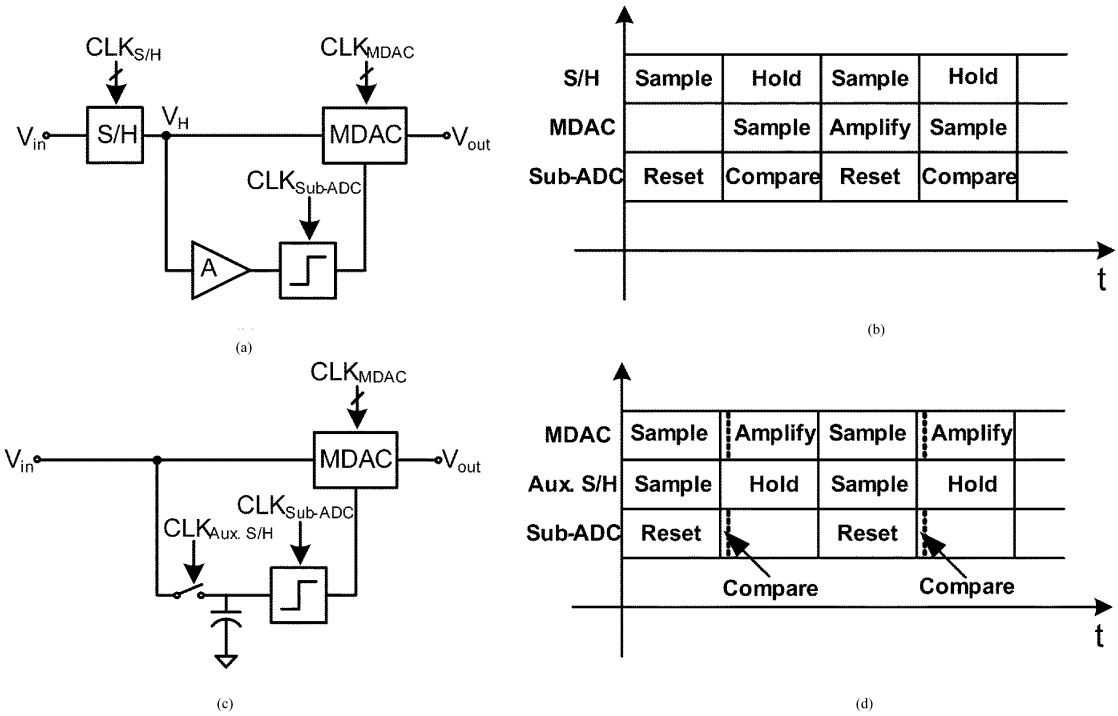

Fig. 2. (a) Block diagram of the first stage of a conventional pipeline ADC with a dedicated front-end S/H and preamplifier (A) in the sub-ADC and (b) the associated operation sequence. (c) Block diagram of the proposed pipeline stage with auxiliary S/H circuit and (d) its operation sequence.

version ϕ_{1d}, which are used to minimize charge injection and clock feedthrough and ensure accurate sampling, as shown in Fig. 1(c). At the top level, the stages receive clock signals in reverse order, so that the clock signal edges advance slightly along the pipeline stages. This ensures that a succeeding stage always samples the correct residue signal from the preceding stage.

B. Auxiliary S/H for Sub-ADC Path

The conventional circuit architecture for the first stage of a pipeline ADC includes a dedicated front-end SHA, as shown in Fig. 2(a), to guarantee that the MDAC path and the sub-ADC path operate on the same sample of the input signal. As shown in Fig. 2(b), the sub-ADC decides while the MDAC is sampling and the sub-ADC outputs are ready when the MDAC starts amplifying. Additionally, preamplifiers are typically used in the comparators of the sub-ADC to block their kickback noise [17]. These approaches allow a fast operation of the ADC, but at the cost of a dedicated front-end SHA circuit and comparator preamplifiers.

Design techniques for signal path SHAs at ultra-low voltages have been explored in [18]. In this study, we propose an architectural change to avoid the front-end SHA, as well as the comparator preamplifiers. As shown in Fig. 2(c), a simple coarse auxiliary S/H is inserted into the sub-ADC path instead. This auxiliary S/H samples the input signal during the same sampling phase as the MDAC path. It holds the input signal while the comparators in the sub-ADC make their decision at the start of the MDAC's residue amplification phase [see Fig. 2(d)]. The auxiliary sampling clock and the comparison clock are nonoverlapping, so that the sampling switch is open during the comparator operation and the comparator regeneration and reset kickback noise are blocked from entering the signal path. In the presented 10-Ms/s pipelined ADC design, the latched comparators, using the topology presented in [19], reach their decision in less than 2% of the sampling clock period, which leaves plenty of time for the MDAC to amplify the residue.[1] The auxiliary S/H can be significantly less accurate than a front-end SHA, since sampling errors are equivalent to comparator offset and a 1.5 bit/stage pipelined ADC is very robust against such offsets.

A mismatch between the time constants of the sampling network in the MDAC path and sub-ADC path translates into an offset in the sub-ADC path [20], [21]. Assuming that the sampling clock skew between these two paths can be neglected, the worst case mismatch error is [20]

$$V_{\text{error}} = A2\pi f_{\text{in}}(\tau_{\text{MDAC}} - \tau_{\text{sub-ADC}}) \tag{1}$$

where A is the full-scale single-ended input-signal amplitude and f_{in} is the maximum signal frequency. τ is defined as the sampling time constant or propagation delay

$$\tau = \frac{\tan^{-1}(2\pi f_{\text{in}} RC)}{2\pi f_{\text{in}}} \approx RC \tag{2}$$

where *RC* is the time constant of the sampling network; since the sampling network bandwidth $(1/RC)$ is designed to be much higher than maximum input frequency f_{in}, the approximation in (2) holds. In the presented ADC, A is equal to $\mathrm{V_{ref}}$, which is 100 mV, and the 1.5 bit sub-ADC can tolerate an offset up

[1]To further improve the design, the nonoverlapping time between the sampling and amplifying phase of the MDAC could be used to get the comparator outputs ready earlier.

to $V_{ref}/4$, or 25 mV, so that, for a maximum signal frequency of 5 MHz when sampling at 10 Ms/s, we obtain the following requirement:

$$\Delta(RC) \approx \Delta\tau < \frac{V_{ref}}{4V_{ref}} \frac{1}{2\pi f_{in}} \approx 8\,\text{ns}. \quad (3)$$

This derivation assumes there are no other offsets in the sub-ADC path. If we allocate half of the total tolerable offset to the comparators, the system is still able to tolerate a sampling-network time-constant difference between the MDAC and sub-ADC of up to 4 ns.

In the presented design, the *RC* network in the MDAC has a time constant smaller than 4 ns to guarantee the dynamic performance in the presence of nonlinear resistance of the switch, so that, theoretically, the auxiliary S/H could be eliminated. However, it is still used to block the comparator kickback noise and to allow for larger comparator offsets. The auxiliary S/H is realized with the same sampling switch as the MDAC path but a sampling capacitor of about half the size. This sampling capacitor is still large enough so that the channel charge injection and the clock feedthrough from the switch do not affect the sampled voltage significantly.

III. Cascaded Sampling to Combat OFF-Switch Leakage in Nanoscale CMOS

In nanoscale CMOS technologies, subthreshold MOS leakage, MOS gate leakage, and reverse-biased PN junction band-to-band tunneling become more and more significant [22]–[24]. At an ultra-low supply voltage of 0.5 V, MOS gate leakage is substantially reduced since it is exponentially dependent on the gate voltage. The reverse-biased PN junction leakage becomes significant when the reverse biasing voltage exceeds the bandgap voltage, which does not occur with a 0.5-V supply. The main leakage concern in this design is the subthreshold leakage of switches in their OFF state, particularly during the nonoverlapping time between sampling and holding phases, when a capacitor is not connected to any voltage source. This leakage causes signal-dependent distortion in the switched-capacitor S/H circuits.

To illustrate the effect of this leakage, a basic S/H circuit and the associated waveforms are shown in Fig. 3(a) and (b). Due to the subthreshold switch leakage, the output voltage V_{out} is not held constant when S_1 is OFF. In the worst case, assuming a rail-to-rail signal at Nyquist rate, V_{in} changes from V_{dd} to 0 after S_1 turns off; this puts S_1 in weak inversion and saturation. The leakage current increases exponentially for a decreasing threshold voltage V_T. Similar leakage challenges exist in each stage of the pipelined ADC when the S/H switches are OFF. This issue is most severe in the first stage where noise and distortion should be kept well below one LSB of the full ADC.

To overcome this problem, a cascaded sampling technique is proposed to alleviate the switch subthreshold OFF leakage. An extra switch S_2 and an additional smaller hold capacitor C_2 are used in front of the main switch S_1 and capacitor C_1, as shown in Fig. 3(c). Switches S_1 and S_2 operate during the same clock phase, but S_2 is turned off slightly later to ensure that it does not affect the accurate sampling on C_1. An intermediate voltage V_1 is now introduced which is held by the extra capacitor C_2. During the track phase, both switches S_1 and S_2 are ON, and V_{out} and V_1 track V_{in}. In the hold phase, S_1 and S_2 are OFF and enter weak inversion. The difference between V_{out} and V_1 is very small but slowly grows during the hold phase due to the leakage of S_2 [see Fig. 3(d)]. S_1 operates in weak inversion but in the linear region with a very small drain-source voltage V_{ds,S_1}; the channel leakage current of each one of the transistor in S_1 is then

$$I \propto \frac{W}{L}\exp\left(\frac{-V_T}{nkT/q}\right)\left[1-\exp\left(\left(\frac{-V_{ds,S_1}}{kT/q}\right)\right)\right] \approx 0 \quad (4)$$

where W/L is the aspect ratio of the transistor, kT/q is the thermal voltage, n is the slope factor, and V_T is transistor threshold voltage. Since V_{ds,S_1} remains very small, the OFF current in S_1 is very small and V_{out} is kept close to constant during the hold phase. The simulation results in Fig. 3(e) show that the slope of the output voltage for the cascaded S/H is about one tenth of the slope for the conventional one. In the worst case leakage scenario, when the transistors are in the fast–fast process corner and operate at a temperature of 85 °C, the proposed sampling circuit still has a leakage rate that is four times lower.

Since there are now two switches in series, the switch size needs to be increased. The extra sampling capacitor C_2 can be kept much smaller than sampling capacitor C_1 to limit the area overhead and settling time impact. C_2 was set to $1/4$ C_1 or 250 fF in this design. The leakage caused by the path connecting to V_{DAC} during the nonoverlap period, does not introduce distortion since the reference voltages are constant.

Switch nonidealities result in important error contributions including settling errors, charge-injection errors, and clock-feedthrough errors. The fully differential circuit topology largely eliminates the latter two, but the voltage-dependent gate capacitance causes slightly different errors in the two differential paths. A switch design using a CMOS transmission gate with half-sized dummy switches was adopted to largely suppress clock feedthrough and charge injection. To reduce the switch threshold voltage and improve settling during the ON state, the switch-transistor gate and body terminals are shorted and connected to the clock signal [18]. With a supply of only 0.5 V, latch-up due to the forward-biased body junction is not a concern [25].

IV. 0.5-V OTA Design

The residue amplifier is the most important active block in a pipelined ADC design. To achieve 8-bit resolution, the OTA DC gain in the first pipeline stage should exceed 50 dB. Assuming a feedback factor of 1/3, which takes into account the input parasitic capacitance of the OTA, the GBW should be at least 18 MHz to achieve a settling accuracy better than 0.4 % for a 10 MHz sampling frequency.

A two-stage OTA with Miller compensation has been designed, as shown in Fig. 4. The first stage (M_1-M_6) uses a folded cascode topology to achieve higher gain, and a common-source second stage (M_7-M_8) is adopted to further increase the gain and to maximize the available output swing. The input and output common-mode voltages are set to 250 mV. In advanced CMOS technology, the threshold voltage can be reduced by

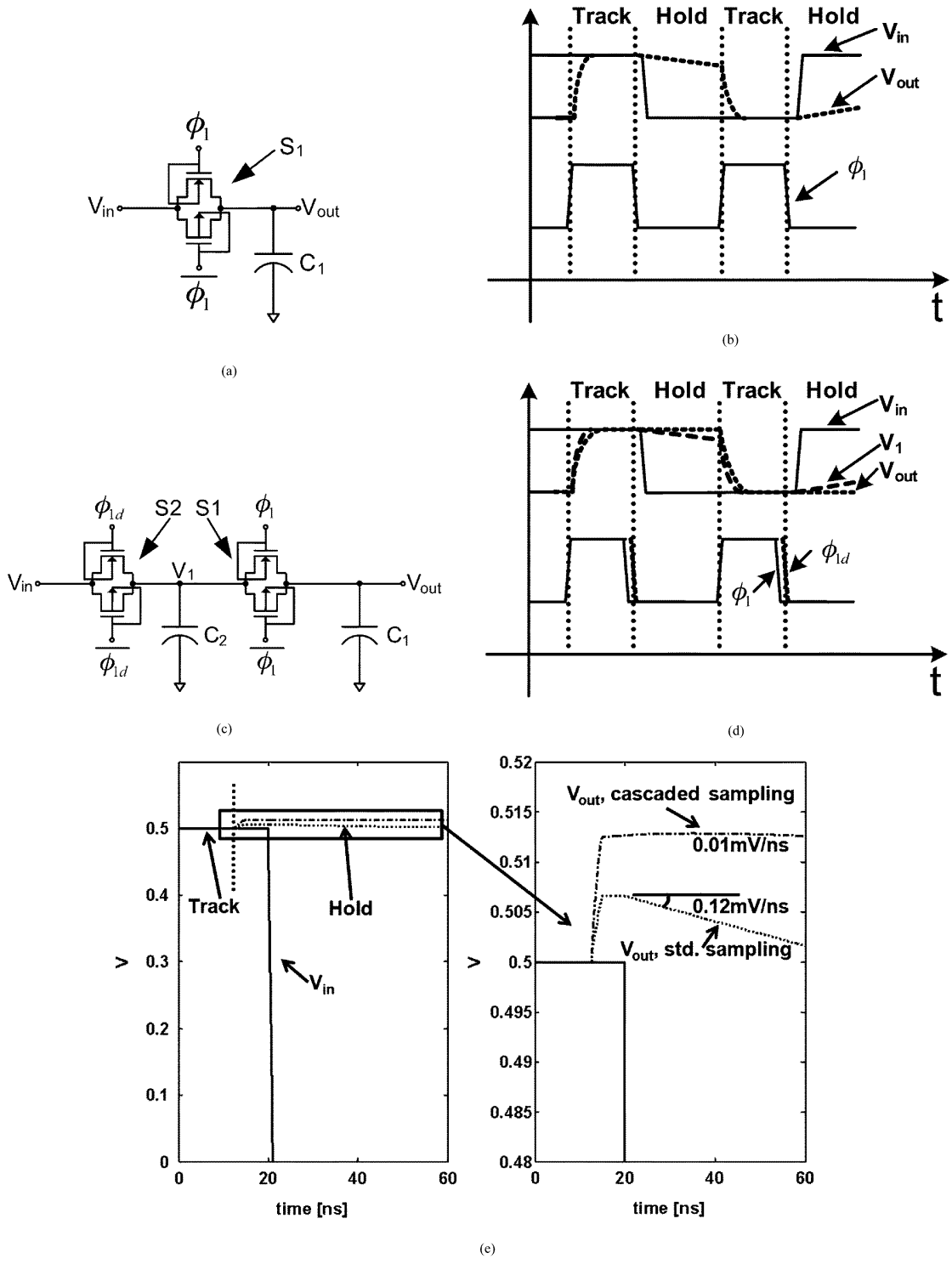

Fig. 3. (a) Standard S/H circuit (all transistors are sized as 12 μm/0.36 μm and C1 is 1pF) and (b) associated node waveforms. (c) Proposed cascaded S/H circuit to combat switch OFF leakage (all transistors are sized as 12 μm/0.36 μm, C1 is 1pF, and C2 is 0.25pF) and (d) associated node waveforms. (e) Simulation results for a rail-to-rail input showing the significant reduction of the effect of leakage during the hold time for the cascaded S/H compared with a standard S/H.

increasing transistor length, which is known as reverse short channel effect (RSCE) [13]. At the same time, the output impedance is also improved. The majority of the transistors in the OTA are sized four times the minimum length or 0.36 μm and have a $\mathrm{V_T}$ between 100 and 200 mV across corners in simulation. The input differential pair transistors $\mathrm{M_{2A}}/\mathrm{M_{2B}}$ have a length of only two times $L_{\min}$ to reduce their parasitic gate-source capacitance which affects the feedback factor; they are biased in weak inversion to maximize their (gm/I) and reduce their $\mathrm{V_{GS}}$ to leave sufficient headroom for the tail current source $\mathrm{M_1}$.

The OTA has a minimum single-ended output swing of 200 $\mathrm{mV_{p\text{-}p}}$. The second stage has a gain larger than 20 dB (in simulation across corners) which results in a 20 $\mathrm{mV_{p\text{-}p}}$

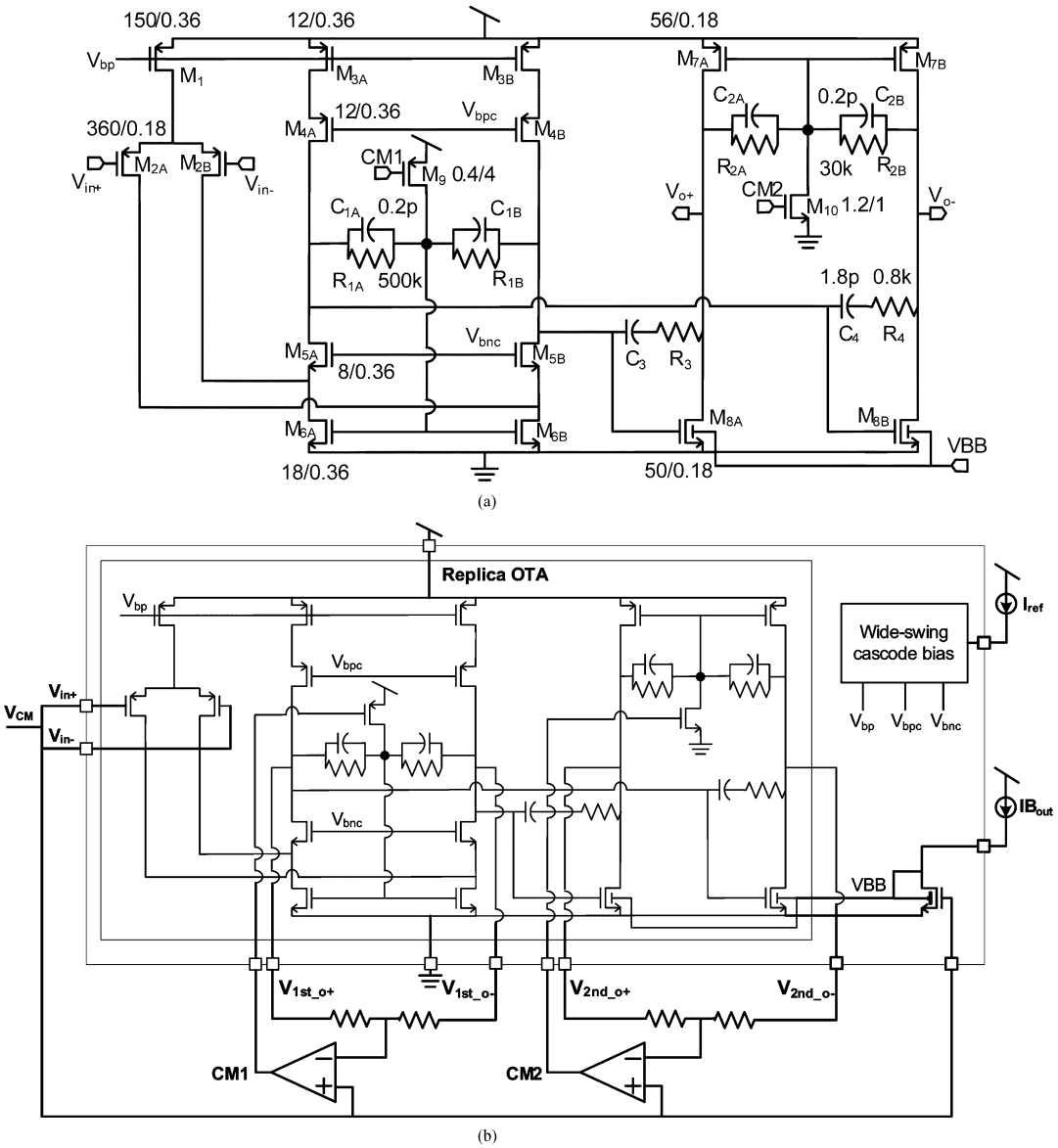

Fig. 4. (a) Schematic of the 0.5-V OTA. Device sizes shown in the schematic have a unit of μm/μm and transistors in symmetrical paths share the same aspect ratio. The bodies of all transistors are shorted to their source terminals, except for the bodies of $\mathrm{M_{8A}}$ and $\mathrm{M_{8B}}$. (b) Overview of the generation of the OTA bias voltages using an on-chip replica OTA.

single-ended signal swing at the output of the first stage. In order to stack four transistors ($\mathrm{M_3}$-$\mathrm{M_6}$) in the cascode stage, their overdrive voltage ($\mathrm{V_{GS}} - \mathrm{V_T}$) was designed to be around 100 mV, resulting in a $\mathrm{V_{DS,sat}}$ of about 80 mV. For a 0.5 V supply and a 20 $\mathrm{mV_{p\text{-}p}}$ single-ended signal swing, each transistor in the stack can be allocated a nominal $\mathrm{V_{DS}}$ of 120 mV, which guarantees operation in the saturation region.

Two local common-mode feedback loops have been adopted so that the output common mode of each stage is set to 250 mV. A single common-mode feedback loop for the full OTA is not suitable, since the output common-mode voltage of the first stage would change too much due to process, voltage, and temperature (PVT) variations and affect the operation of the cascode transistors M3-M6. Local common-mode feedback further offers easier control of the loop dynamics and stability. In each stage, common-mode sensing resistors ($\mathrm{R_{1A}}$ and $\mathrm{R_{1B}}$, $\mathrm{R_{2A}}$ and $\mathrm{R_{2B}}$) feed back the common-mode signals to the gates of the active loads. Shunt capacitors ($\mathrm{C_{1A}}$ & $\mathrm{C_{1B}}$, $\mathrm{C_{2A}}$ & $\mathrm{C_{2B}}$) improve the high-frequency common-mode feedback and maintain the common-mode gain well below 0 dB at higher frequencies. $\mathrm{M_9}$ and $\mathrm{M_{10}}$ push a small DC current through the resistors to generate a voltage drop that determines the DC output common-mode voltages. The appropriate bias voltages for nodes CM1 and CM2 to set the level shift currents and maintain the common-mode voltages at 250 mV across PVT variations are generated on-chip using servo loops across a replica OTA, as shown in Fig. 4(b). For testing flexibility, the servo-loop error amplifiers were implemented on the PCB test board. The $\mathrm{V_{GS}}$ of the output transistors $\mathrm{M_{8A}}/\mathrm{M_{8B}}$ is kept at 250 mV by the common-mode biasing and, due to PVT variations, the current in the output stage is not well controlled. An on-chip bias circuit, also shown in Fig. 4(b), adjusts the body voltage of the output transistors to control their DC bias current. The bias voltages $\mathrm{V_{bp}}$, $\mathrm{V_{bpc}}$, and $\mathrm{V_{bnc}}$ are generated on-chip using standard wide-swing cascode biasing circuits. Each of these bias circuits is implemented once on the prototype

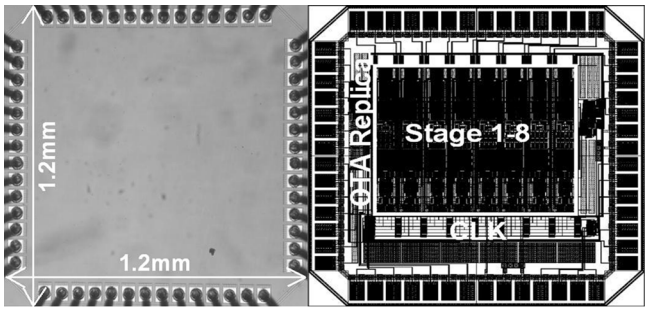

Fig. 5. Die photo (left) and layout plot (right).

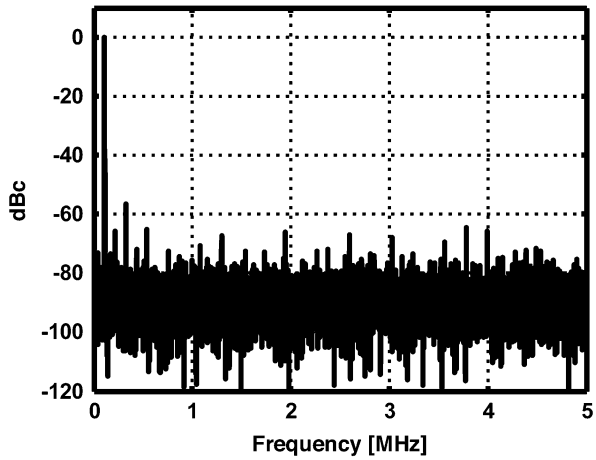

Fig. 6. Measured output spectrum at 10 Ms/s with a full-scale 109-kHz sinewave input using a 16384-point FFT.

chip and is shared by all stages; they have been laid out next to the first stage in the pipeline since its requirements are most stringent.

The measured performance of the replica OTA on our prototype chip was a DC gain of 50 dB and a GBW of 32 MHz for a differential load of 3 pF. Each OTA draws 530 μA under nominal conditions.

V. Experimental Results

The die photograph and layout of the chip prototype is shown in Fig. 5. It was fabricated in a 90 nm CMOS technology using regular V_T devices. The chip size is 1.2 mm $\times$ 1.2 mm and the active area is 0.95 mm $\times$ 0.9 mm. The chip is covered by metal 9 fill structures; the main chip sections are shown on the layout: eight identical pipeline stages, the clock generator and buffer, and the OTA replica biasing.

The dies were packaged in a 64-pin QFP package and mounted on a circuit board which included the external voltage reference generators and the error amplifiers for the biasing loops. A Tektronix AWG2021 arbitrary waveform generator provided the differential input signals, and an Agilent 33220A generated the input clock. An Agilent 1692AD logic analyzer collected the uncorrected bits from all the stages. The digital offset correction was performed offline.

Fig. 6 shows the digital output spectrum for a full-scale 109-kHz input signal while operating from a 0.5-V supply and sampling at 10 Ms/s. The third-order harmonic is 57 dB

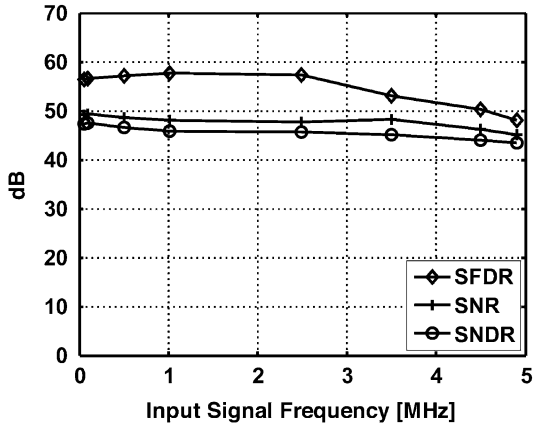

Fig. 7. Measured SNDR, SNR, and SFDR at 10 Ms/s for a full-scale input sinewave with frequencies varying from 101 kHz to 4.9 MHz.

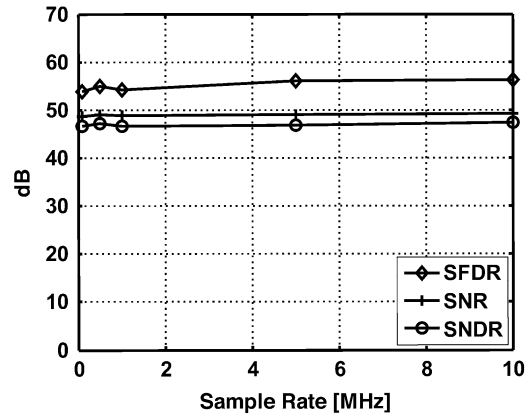

Fig. 8. Measured SNDR, SNR, and SFDR for a full-scale input sinewave at 49 kHz with sampling frequencies varying from 100 kHz to 10 MHz.

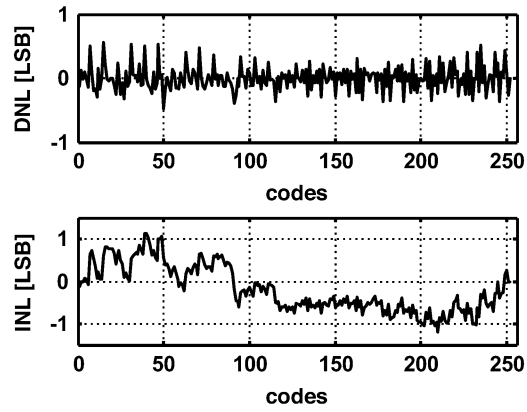

Fig. 9. Measured DNL and INL.

below the signal. This distortion is probably due to the finite gain of the OTA in the residue amplifier or possibly due to capacitor mismatch. The signal-to-noise ratio (SNR), the signal-to-noise-and-distortion ratio (SNDR), and the spurious-free dynamic range (SFDR) for full-scale input signals with frequencies ranging from 101 kHz to 4.9 MHz are shown in Fig. 7; the dynamic performance of the converter is quite flat with about a 4-dB drop in the SNDR at the Nyquist frequency. This illustrates the effectiveness of the adopted pipeline stage

TABLE I
ADC PERFORMANCE SUMMARY ($T = 27°C$)

Resolution	8			bits
Sample Rate	10			Msps
Full Scale Input Signal Range	0.4			$V_{pp,\,diff}$
VDD	0.45	0.5	0.55	V
SNDR*	46.8	48.1	47.2	dB
SNR*	48.4	49.3	48.9	dB
SFDR*	55.1	57.2	56.5	dB
DNL min/max	-0.54/0.65	-0.48/0.55	-0.59/0.85	LSB
INL min/max	-1.6/0.89	-1.19/1.12	-1.8/1.1	LSB
Power	2.3	2.4	2.6	mW
Die Size	1.2 x 1.2			mm^2
Technology	90 nm CMOS with regular VT devices			

*Measured with a 109 kHz, full scale, sinusoidal input signal.

topology using an additional coarse sub-ADC S/H while eliminating the front-end SHA.

The ADC's SNR, SNDR, and SFDR are very consistent for sampling frequencies ranging from 100 kHz to 10 MHz, as shown in Fig. 8. This demonstrates that the switch leakage of the cascaded sampling circuit is not significant even at 100 ks/s. The static performance of the ADC was determined by taking 2048 samples at 10 Ms/s of a full-scale ramp input signal and is shown in Fig. 9; the maximum $|\mathrm{DNL}|$ and $|\mathrm{INL}|$ is 0.55 and 1.19 LSB, respectively.

Table I summarizes the measured results including the performance for $\pm 10\%$ supply voltage variations; the performance is consistent from 0.45 to 0.55 V, with less than 1.9 dB difference. The chip was further tested at 80 °C, and a degradation of less than 3 dB in the SNDR degradation was observed for 0.5 V and 10 Msps operation. The pipelined ADC has eight identical stages, nominally consumes 2.4 mW from a 0.5 V supply, and has a figure of merit is 1.15 pJ/Conv. Ten chip samples were tested, and the variation in their SNDR performance was within a ± 0.75 dB range.

VI. CONCLUSION

A 0.5-V 8-bit 10-MS/s pipelined ADC has been realized using a 90 nm standard CMOS technology. A cascaded sampling technique was introduced to combat the switch OFF leakage. The separate front-end SHA in conventional topologies has been eliminated by adding an auxiliary S/H circuit for the sub-ADC path to the pipeline stage topology and by synchronizing the sampling of the pipeline residue amplifier and sub-ADC. A 0.5-V two-stage OTA with replica biasing and output current control has been designed. Throughout the design, the V_T reduction thanks to the RSCE has been used to optimize the device sizing and operation and to enable high-performance analog/mixed-signal design for ultra-low supply voltages. The presented prototype has eight identical stages and achieves a conversion efficiency of 1.15 pJ/conversion.[2] This prototype demonstrates that true low-voltage pipelined ADCs operating from 0.5-V are feasible in nanoscale CMOS technologies without resorting to special devices or voltage-boosting techniques.

[2]In a redesign, instead of using identical stages as in the presented prototype, progressive size and power scaling can be used which can improve the efficiency of this pipelined ADC to below 0.5pJ/conversion.

ACKNOWLEDGMENT

The authors would like to thank S. Ranganathan and S. Chatterjee for insightful discussions on the cascaded sampling technique, and N. Stanic for designing the interdigitated capacitor which was simulated using the EMX tool donated by Integrand Software.

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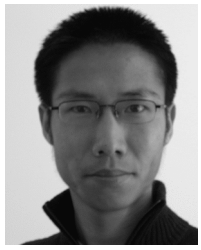

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